PCI-FRM01 Register Level Application Guide (Ver1.1)

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References

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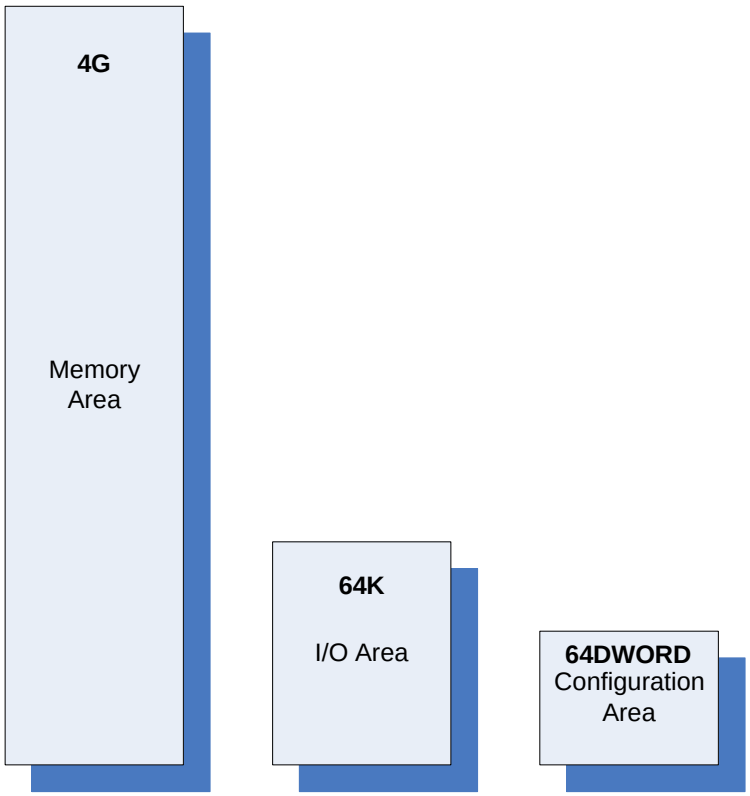
1. PCI BUS Address Space

As it uses CPU of the x86 system which we use mainly, it can classify greatly it to memory and I/O area. In order to support Plug & Play in case of PCI bus that has a special configuration. It can make the resource and device state control register etc.



The PCI-FRM01 use a memory and I/O that have been assigned to system for operation, the contents are as follows that they required.

Address Area	Requirements	Remark
Memory	Maximum 64MByte	
I/O	256 Byte	
Configuration	128 Byte	

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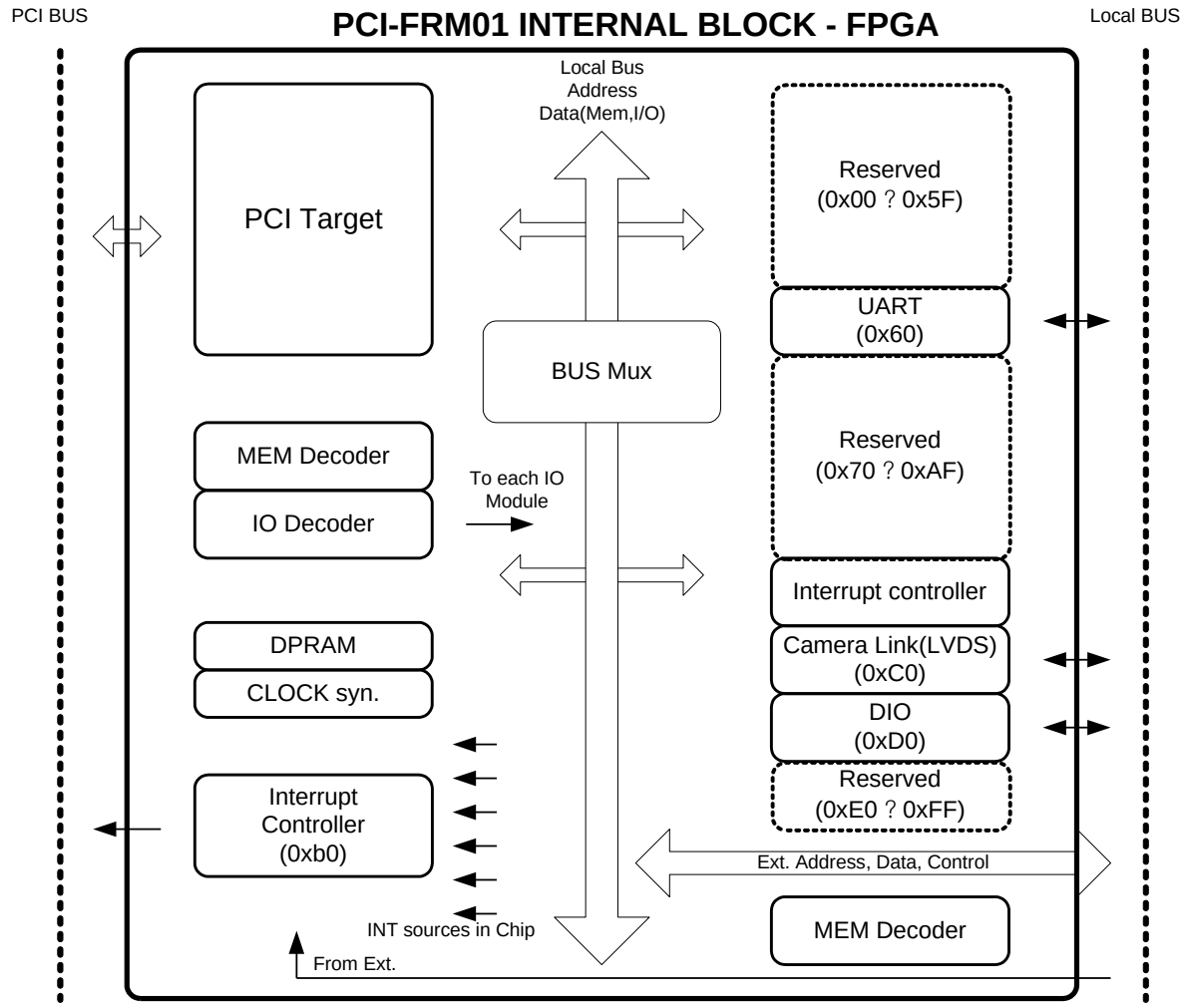
2. PCI-FRM01 Functional Block Diagram

The address area assigned by the system in the PCI-FRM01 division is shown in the figure below. Most peripheral control and status register is in the I/O area, only SDR SRAM is in the memory area. The configuration area can not be used in the most application because of only using resources for the system boot time.



PCI-FRM01 of the figure shows the function block, which features the dotted area is reserved for future feature additions.

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3. I/O Address Usage

The below table indicates the base address of the peripheral device that is located I/O area address.

The table below the I / O area is located at the address indicates the base address of the peripheral device. All I / O registers are 32-bit input / output processing.

I/O Address Offset Base	Function	Description	Comment
00h-5Fh	Reserved	Reserved area for future use	
60h	UART	Universal asynchronous receiver transmitter (RS232C)	
70h-AFh	Reserved	Reserved area for future use	
B0h	Interrupt	Interrupt controller	
C0h	Camera Link	Frame grabber LVDS interface	
D0h	DIO	Photo-coupler isolated Digital input/Output	
E0h-FFh	Reserved	Reserved area for future use	

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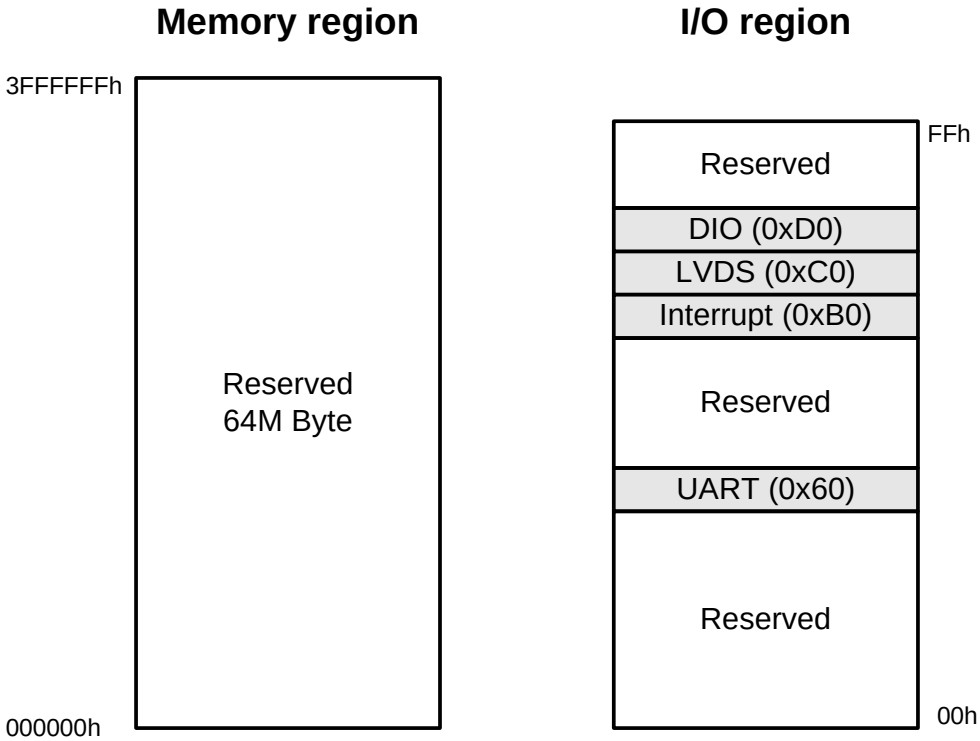
4. Memory Address Usage

SDR SRAM for future enhancements can be used.

Memory Address Space	Model	Description	Comment
0h - 4000000h	Undefined	SDR SDRAM 64M Byte	Reserved



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5. UART Usage

The PCI-FRM01 has UART (9600BPS, 1 stop, 1 start, 8 data bit, no parity).

Function	I/O Address Offset	Register	Description
UART	60h	Data Buffer	Transmit Data(Write) / Received Data(Read)
	64h	Baud	Baud generator x"82"
	68h	Control	Control Register
	6Ch	Status	Status Register

(1) Data Buffer

(2) Baud rate generator

40Mhz

Initial Value : x"82"

(3) Control

UART Control Register Bit Position & Usage

31 ~ 8	7	6	5	4	3	2	1	0
Reserved							TE	RE

Bit	Name	Description	Default Value
0	RE	Receiver Interrupt Enable	'0'
1	TE	Transmitter Interrupt Enable	'0'
31 - 2	Reserved	For future use	All '0'

(4) STATUS

UART STATUS Register Bit Position & Usage

31 ~ 8	7	6	5	4	3	2	1	0
Reserved			TB	TI	FE	PE	RB	RI

Bit	Name	Description	Default Value
0	RI	Receive Interrupt	'0'
1	RB	Receive Busy	'0'
2	PE	Parity Error(Unused)	'0'

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3	FE	Frame Error	'0'
4	TI	Transmit Interrupt	'0'
5	TB	Transmit Busy	'0'
31 - 2	Reserved	For future use	All '0'

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6. Interrupt Controller Usage

PCI-FRM01 has interrupt controller to handle the hardware interrupt for each I/O device.

When you use these interrupts, eliminating the use of polling overhead of the process can be reduced.

Function	I/O Address Offset	Register	Description
INTERRUPT	B0h	INT_STA	Interrupt Status Register (Read Only)
	B4h	INT_SEL	Interrupt Status Clear (Write Only)
	B8h	INT_EN	Interrupt Enable Register (Read/Write)
	BCh	INT_SRC	Interrupt Source Indication(Read Only)

To control 82C55 ports, first the mode have to set up through the control register. To all setup, most significant bit(MSB) is set to high “1” and write to the control register. If the MSB is “0”, it will be command of PORTC. (For more information, refer 82C55 manual)

When the first time power is applied, all ports will be the input and operation modes will be 0.

(1) INT_STA (Interrupt Status)

Indicates the current interrupt device that requires. To appear in the status register will have to make the handle. When the write operation, status bits are cleared.

INTERRUPT Status Register Bit Position & meaning																
31	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		G	S14								Status						S0

Bit	Name	Description	Default Value
0		Reserved	‘0’
1		Reserved	‘0’
2		Reserved	‘0’
3		Reserved	‘0’
4		Reserved	‘0’
5		Reserved	‘0’
6	UART	Differential RS232C interface	‘0’
7		Reserved	‘0’
8		Reserved	‘0’
9		Reserved	‘0’
10		Reserved	‘0’

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11	Interrupt	Reserved	'0'
12	LVDS	Reserved	'0'
13		Reserved	'0'
14		Reserved	'0'
15	Global	When any of the above interrupt sources need the processing, it will be changed '1'.	'0'
31-16	Reserved	For future use	All '0'

For more information, refer AD5324 manual.

(2) INT_SEL

Select the Level Trigger and Edge Trigger of Interrup Input.

INTERRUPT Clear Register Bit Position & meaning																
31 16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	R	C14							Status Clear							C0

If it is "0", it is a Level Trigger. If it is "1", it is a Rising Edge Trigger.

(3) INT_EN

Each interrupt source is to enable the interrupt.

INTERRUPT Enable Register Bit Position & meaning																
31 16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	G	E14							Enable							E0

If each bit is '1', the device interrupt for corresponding bit will be enabled.

The bit 15 is Global Interrupt Enable. This bit is set to '1' to enable all interrupts.

(4) INT_SRC

INT_STA appear on the register, the interrupt request output of the device is latched at the rising edge of the signal. Thus, it is not Level Trigger, it is an indication of Edge Triggere.

So, it can be cleared and requested the interrupt. On the other hand, in the INT_SRN, it represents current output signal state of the current device.

INTERRUPT Source Indicator Bit Position & meaning															
31 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	S14							Interrupt Source							S0

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7. LVDS(Camera Link) Interface Usage

LVDS(Low Voltage Differential Signal) Interface control

Function	I/O Address Offset	Register	Description
LVDS	C0h	LVDS_DATA	LVDS Data register
	C4h	LVDS_CMD	LVDS Command register
	C8h	LVDS_CNT	LVDS Internal counter register
	CCh	LVDS_STA	LVDS Status register

LVDS Data Register Bit Position & meaning

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D31																Data															D0

LVDS Command Register Bit Position & meaning

31	5	4	3	2	1	0
Reserved		S	I	D	R	E

Bit	Name	Description	Default Value
0	Enable	Used for simulation	'0'
1	Reset		'0'
2	Data Enable		'0'
3	Interrupt Enable		'0'
4	Start		'0'

LVDS Internal counter Register Bit Position & meaning

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P15								Pixel Counter							P0	L15								Line Counter							L0

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LVDS Status Register Bit Position & meaning																												
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
V	H	R		LVDS Address												I	F	L	R	D	A10	PC Address									A0

Bit	Name	Description	Default Value
10-0	PC address	Dual port ram address	
11	Done		'0'
12	Data Ready		'0'
13	Lvalid		'0'
14	Fvalid		'0'
15	Interrupt		'0'
27-16	LVDS address	Dual port ram address	
28	Reserved		
29	Data ready		'0'
30	Hsync		'0'
31	Vsync		'0'

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8. DIO(Digital Input/Output) Usage

The PCI-FRM01 has 16 Input port and 8 Output port at the Photo-coupler isolated DIO(Digital Input/Output) function.

Function	I/O Address Offset	Register	Description
DIO	D0h	Out Port	4Bit Photo-coupler output, 4Bit LVDS output Port
	D4h	In Port	6Bit Photo-coupler input , 10Bit LVDS input Port
	D8h	Reserved	For future use
	DCh	Reserved	For future use

DIO Out Port Register Bit Position & Usage									
31 ~ 4	7	6	5	4	3	2	1	0
Reserved	Used							

Bits 3-0 are the Photo-coupler isolated Digital outputs, bits 7-4 are the LVDS outputs. Please refer to the manual for the circuit configuration.

DIO In Port Register Bit Position & Usage																
31 ~ 16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	Used															

Bits 5-0 are the Photo-coupler isolated Digital Inputs, bits 15-8 are the LVDS Inputs. Please refer to the manual for the circuit configuration.

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References

1. Specifications of the Camera Link Interface Standard for Digital Cameras and Frame Grabbers

-- PULNix America, Inc.

2. Channel Link Design Guide

-- National Semiconductor

3. PCI-EK01(A/B) User's Manual

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4. DS90CR285/286 chip manual

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5. PCI-FRM01 User's manual

-- DAQ system

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